annotated task graph
Terms used: annotated task graph
Found

Sort results by relevance
Display results expanded form
Save results to a Binder
Open results in a new window

Refine these results with Advance
Try this search in The ACM Guide

Results 1 - 20 of 2,479 Result page: 1 2 3 4 5 6 7 8 9 10 next >>

1 Time-Energy Design Space Exploration for Multi-Layer Memory Architectures
Radoslaw Szymanek, Francky Catthoor, Krzysztof Kuchcinski
February 2004 DATE '04: Proceedings of the conference on Design, automation and test in Europe - Volume 1 Volume 1
Publisher: IEEE Computer Society
Full text available: Pdf (203.40 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 6, Citation Count: 3

This paper presents an exploration algorithm which examines execution time and energy consumption of a given application, while considering a parameterized memory architecture. The input to our algorithm is an application given as an annotated task graph ...

2 MILP based task mapping for heterogeneous multiprocessor systems
A. Bender
September 1996 EURO-DAC '96/ EURO-VHDL '96: Proceedings of the conference on European design automation
Publisher: IEEE Computer Society Press
Full text available: Pdf (129.08 KB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 50, Citation Count: 9

3 Joint throughput and energy optimization for pipelined execution of embedded streaming applications
Po-Kuan Huang, Matin Hashemi, Soheil Ghiasi
July 2007 ACM SIGPLAN Notices, Volume 42 Issue 7
Publisher: ACM
Full text available: Pdf (147.11 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 65, Citation Count: 0

We present a methodology for synthesizing streaming applications, modeled as task graphs, for pipelined execution on multi-core architectures. We develop a task graph extraction and characterization framework that accurately determines the structure, ...

Keywords: embedded soft-ware synthesis, multi-core, performance optimization, task graph

4 Joint throughput and energy optimization for pipelined execution of embedded streaming applications
Po-Kuan Huang, Matin Hashemi, Soheil Ghiasi

June 2007 LCTES '07: Proceedings of the 2007 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems
Publisher: ACM
Full text available: Pdf (147.11 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 65, Citation Count: 0

We present a methodology for synthesizing streaming applications, modeled as task graphs, for pipelined execution on multi-core architectures. We develop a task graph extraction and characterization framework that accurately determines the structure, ...

Keywords: embedded soft-ware synthesis, multi-core, performance optimization, task graph

5 Embedded System Design Based On Webservices
A. Rettberg, W. Thronicke
March 2002 DATE '02: Proceedings of the conference on Design, automation and test in Europe
Publisher: IEEE Computer Society
Full text available: Pdf (288.51 KB) Additional Information: full citation, abstract

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 53, Citation Count: 0

The structure of Internet applications andscenarios is changing rapidly today. This offersnew potential for established technologies andmethods to expand their area of application. Newtechnologies encourage new methodologies todesign processes and business-to-businessapplications. ...

6 Interactive schedulability analysis
Unmesh D. Bordoloi, Samarjit Chakraborty
December 2007 ACM Transactions on Embedded Computing Systems (TECS), Volume 7 Issue 1
Publisher: ACM
Full text available: Pdf (434.12 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 171, Citation Count: 0

A typical design process for real-time embedded systems involves choosing the values of certain system parameters and performing a schedulability analysis to determine whether all deadline constraints can be satisfied. If such an analysis returns a negative ...

Keywords: Schedulability analysis, interactive design, nonfunctional constraints, performance debugging, recurring real-time task model

7 Real-time video content analysis: QoS-aware application composition and parallel processing
Viktor S. Wold Eide, Ole-Christoffer Granmo, Frank Eliassen, Jørgen Andreas Michaelsen
May 2006 ACM Transactions on Multimedia Computing, Communications, and Applications (TOMCCAP), Volume 2 Issue 2
Publisher: ACM
Full text available: Pdf (393.86 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 24, Downloads (12 Months): 200, Citation Count: 0

Real-Time content-based access to live video data requires content analysis applications that are able to process video streams in real-time and with an acceptable error rate. Statements such as this express quality of service (QoS) requirements. In ...

Keywords: QoS and resource management, Real-Time video content analysis, event-based communication, parallel processing, publish/subscribe, task graph scheduling

8 Declarative Ajax and client side evaluation of workflows using iTasks
Rinus Plasmeijer, Jan Martin Jansen, Pieter Koopman, Peter Achten
July 2008 PPDP '08: Proceedings of the 10th international ACM SIGPLAN conference on Principles and

practice of declarative programming
Publisher: ACM
Full text available: Pdf (757.94 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 21, Citation Count: 0

Workflow systems coordinate tasks of humans and computers. The iTask system is a recently developed toolkit with which workflows can be defined declaratively on a very high level of abstraction. It offers functionality which cannot be found in commercial ...

Keywords: Ajax, SapI, clean, generic programming, iData, iTask, web programming, workflow systems

9 Supporting timeliness and accuracy in distributed real-time content-based video analysis
Viktor S. Wold Eide, Frank Eliassen, Ole-Christoffer Granmo, Olav Lysne
November 2003 MULTIMEDIA '03: Proceedings of the eleventh ACM international conference on Multimedia
Publisher: ACM
Full text available: Pdf (339.39 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 59, Citation Count: 5

Real-time content-based access to live video data requires content analysis applications that are able to process the video data at least as fast as the video data is made available to the application and with an acceptable error rate. Statements as ...

Keywords: QoS and resource management, event-based communication, parallel processing, real-time video content analysis, task graph scheduling

10 Robust and sustainable schedulability analysis of embedded software
Madhukar Anand, Insup Lee
June 2008 LCTES '08: Proceedings of the 2008 ACM SIGPLAN-SIGBED conference on Languages, compilers, and tools for embedded systems
Publisher: ACM
Full text available: Pdf (468.10 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 48, Citation Count: 0

For real-time systems, most of the analysis involves efficient or exact schedulability checking. While this is important, analysis is often based on the assumption that the task parameters such as execution requirements and inter-arrival times between ...

Keywords: robust schedulability analysis, schedulability analysis, sustainable schedulability analysis

11 Robust and sustainable schedulability analysis of embedded software
Madhukar Anand, Insup Lee
June 2008 ACM SIGPLAN Notices, Volume 43 Issue 7
Publisher: ACM
Full text available: Pdf (468.10 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 48, Citation Count: 0

For real-time systems, most of the analysis involves efficient or exact schedulability checking. While this is important, analysis is often based on the assumption that the task parameters such as execution requirements and inter-arrival times between ...

Keywords: robust schedulability analysis, schedulability analysis, sustainable schedulability analysis

12 Optimal integration of inter-task and intra-task dynamic voltage scaling techniques for hard real-time applications

Jaewon Seo, Taewhan Kim, N. D. Dutt
May 2005 ICCAD '05: Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design
Publisher: IEEE Computer Society
Full text available: Pdf (260.86 KB) Additional Information: full citation, abstract, references, cited by

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 35, Citation Count: 4

It is generally accepted that the dynamic voltage scaling (DVS) is one of the most effective techniques for energy minimization. According to the granularity of units to which voltage scaling is applied, the DVS problem can be divided into two subproblems: ...

13 The worst-case execution-time problem—overview of methods and survey of tools
Reinhard Wilhelm, Jakob Engblom, Andreas Ermedahl, Niklas Holsti, Stephan Thesing, David Whalley, Guillem Bernat, Christian Ferdinand, Reinhold Heckmann, Tulika Mitra, Frank Mueller, Isabelle Puaut, Peter Puschner, Jan Staschulat, Per Stenström
April 2008 ACM Transactions on Embedded Computing Systems (TECS), Volume 7 Issue 3
Publisher: ACM
Full text available: Pdf (856.48 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 82, Downloads (12 Months): 310, Citation Count: 1

The determination of upper bounds on execution times, commonly called worst-case execution times (WCETs), is a necessary step in the development and validation process for hard real-time systems. This problem is hard if the underlying processor architecture ...

Keywords: Hard real time, worst-case execution times

14 CellSs: a programming model for the cell BE architecture
Pieter Bellens, Josep M. Perez, Rosa M. Badia, Jesus Labarta
November 2006 SC '06: Proceedings of the 2006 ACM/IEEE conference on Supercomputing
Publisher: ACM
Full text available: Html (2.09 KB), Pdf (608.33 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 111, Citation Count: 8

In this work we present Cell superscalar (CellSs) which addresses the automatic exploitation of the functional parallelism of a sequential program through the different processing elements of the Cell BE architecture. The focus in on the simplicity and ...

15 Communication-aware stochastic allocation and scheduling framework for conditional task graphs in multi-processor systems-on-chip
Emiliano Dolif, Michele Lombardi, Martino Ruggiero, Michela Milano, Luca Benini
September 2007 EMSOFT '07: Proceedings of the 7th ACM & IEEE international conference on Embedded software
Publisher: ACM
Full text available: Pdf (550.55 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 22, Downloads (12 Months): 162, Citation Count: 0

The increasing levels of system integration in Multi-Processor System-on-Chips (MPSoCs) emphasize the need for new design flows for efficient mapping of multi-task applications onto hardware platforms. Even though data-flow graphs are often used for ...

Keywords: allocation, multimedia dataflow streaming, scheduling

16 Synthesis of an application-specific soft multiprocessor system
Jason Cong, Guoling Han, Wei Jiang

February 2007 FPGA '07: Proceedings of the 2007 ACM/SIGDA 15th international symposium on Field programmable gate arrays
Publisher: ACM
Full text available: Pdf (432.41 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 13, Downloads (12 Months): 161, Citation Count: 0

The application-specific multiprocessor System-on-a-Chip is a promising design alternative because of its high degree of flexibility, short development time, and potentially high performance attributed to application-specific optimizations. However, ...

Keywords: clustering, design space, labeling, multiprocessor, pipeline

17 Partial task assignment of task graphs under heterogeneous resource constraints
Radoslaw Szymanek, Krzysztof Krzysztof
June 2003 DAC '03: Proceedings of the 40th conference on Design automation
Publisher: ACM
Full text available: Pdf (343.44 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Citation Count: 2

This paper presents a novel *partial assignment technique* (PAT) that decides which tasks should be assigned to the same resource without explicitly defining assignment of these tasks to a particular resource. Our method simplifies the assignment ...

Keywords: constraint logic programming, scheduling, task assignment

18 Schedulability analysis of multiprocessor real-time applications with stochastic task execution times
Sorin Manolache, Petru Eles, Zebo Peng
November 2002 ICCAD '02: Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design
Publisher: ACM
Full text available: Pdf (107.76 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 21, Citation Count: 4

This paper presents an approach to the analysis of task sets implemented on multiprocessor systems, when the task execution times are specified as generalized probability distributions. Because of the extreme complexity of the problem, an exact solution ...

19 Scheduling and Timing Analysis of HW/SW On-Chip Communication in MP SoC Design
Youngchul Cho, Ganghee Lee, Sungjoo Yoo, Kiyoung Choi, Nacer-Eddine Zergainoh
March 2003 DATE '03: Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2, Volume 2
Publisher: IEEE Computer Society
Full text available: Publisher Site, Pdf (250.77 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 11, Citation Count: 1

On-chip communication design includes designing software (SW) parts (operating system, device drivers, interrupt service routines, etc.) as well as hardware (HW) parts (on-chip communication network, communication interfaces of processor/IP/memory, on-chip ...

20 LEneS: task scheduling for low-energy systems using variable supply voltage processors
Flavius Gruian, Krzysztof Kuchcinski
January 2001 ASP-DAC '01: Proceedings of the 2001 conference on Asia South Pacific design automation
Publisher: ACM

Full text available: Pdf (112.11 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 54, Citation Count: 37

The work presented in this paper addresses minimization of the energy consumption of a system during system-level design. The paper focuses on scheduling techniques for architectures containing variable supply voltage processors, running dependent tasks. ...

Results 1 - 20 of 2,479 Result page: 1 2 3 4 5 6 7 8 9 10 next >>